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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,514	03/28/2001	William C. Anderson	10559-394001	5444

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,514	ANDERSON ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 10-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-8, and 10-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *12 June 2004* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 3-8, and 10-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 6-7, "said first updated data address value" lacks proper antecedent basis since it was not described. It is suggested to change "said first updated data address value" to - said first data address value -.

In claim 1, lines 9-10, "the second value" lacks proper antecedent basis since it was not described. It is suggested to change "the second value" to - the second data address value-.

In claim 7, lines 1-2, "the first updated data address value" lacks proper antecedent basis since it was not described.

It is suggested to change "the first updated data address value" to -said first data address value-.

In claim 8, line 10, "the pipeline" lacks proper antecedent basis since it was not described.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5-8, 12-17, 20-24, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Murakami et al. (U.S. Patent No. 5,237,667) hereafter referred to as Murakami et al.'667.

Referring to claim 1, Murakami et al.'667 discloses as claimed a method for use in a pipelined processor (see Figs. 24

and 28) including a plurality of stages ((1) Fetch; (2)Decode, and Address Update; (3) Read; (4) Execution; (5) Write/Accumulation, see Fig. 28), the method comprising: storing a first data address value (the entry in Address Register ARX (x: 0-3), see Fig. 44) in a future file (Address Register ARX (x: 0-3), see Fig. 44); and generating (by Adder 534 and 537, see Fig. 44) a second data address value (Feed back Data 538, see Fig. 44) from said first data address value; and updating the future file (Address Register ARX (x: 0-3), see Fig. 44) with the second data address value (Feed back Data 538, see Fig. 44) without terminating an instruction associated with the second value in the pipeline (the pipelined stages: (1) Fetch; (2)Decode, and Address Update; (3) Read; (4) Execution; (5) Write/Accumulation, see Fig. 28).

Referring to claim 8, Murakami et al.'667 discloses as claimed an article comprising a machine-readable medium (inherently existing in Murakami et al.'667's main memory) which stores machine-executable instructions, the instructions causing a machine to store a first data address value (the entry in Address Register ARX (x: 0-3), see Fig. 44) in a future file (Address Register ARX (x: 0-3), see Fig. 44); and generate (by Adder 534 and 537, see Fig. 44) a second data address value (Feed back Data 538, see Fig. 44) from said first data address

value; and updating the future file (Address Register ARX (x: 0-3), see Fig. 44) with the second data address value without terminating an instruction associated with the second value in the pipeline (the pipelined stages: (1) Fetch; (2) Decode, and Address Update; (3) Read; (4) Execution; (5) Write/Accumulation, see Fig. 28).

Referring to claims 15 and 22, Roth et al. discloses as claimed a processor (inherently, the CPU of Murakami et al.'667's system) comprising: a pipeline (see Fig. 28) comprising two or more stages (the pipelined stages: (1) Fetch; (2)Decode, and Address Update; (3) Read; (4) Execution; (5) Write/Accumulation, see Fig. 28); a future file (Address Register ARX (x: 0-3), see Fig. 44) operative to store a one or more data address value; a data address generator (Adder 534 and 537, see Fig. 44) operative to generate an updated data address value (Feed back Data 538, see Fig. 44) from one or more of said data address values, and an update bus connected between the data address generator (Adder 534 and 537, see Fig. 44) and the future file (Address Register ARX (x: 0-3), see Fig. 44) and operative to write the updated data address value to the future file without terminating an instruction associated with the updated value in the pipeline (the pipelined stages: (1) Fetch; (2) Decode, and Address Update; (3) Read; (4) Execution; (5)

Write/Accumulation, see Fig. 28). Regarding claim 22, Murakami et al.'667 also discloses: a processor coupled to a static random access memory (Murakami et al.'667's main memory which is inherently existing).

As to claims 5 and 12, Murakami et al.'667 also discloses: generating the second updated data address value comprises calculating the second updated data address value (Feed back Data 538, see Fig. 44) with a data address generator (Adder 534 and 537, see Fig. 44) in an address calculation stage (Address Update stage, see Fig. 28) of the pipeline.

As to claims 6 and 13, Murakami et al.'667 also discloses: providing the future file (Address Register ARX (x: 0-3), see Fig. 44) in a decode stage ((2) Decode stage, see Fig. 28) of the pipeline.

As to claims 7, 14, 20, and 27, Murakami et al.'667 also discloses: storing the first updated data address value comprises storing at least one of an index value (certainly existing in Address Register ARX (x: 0-3), see Fig. 44 in order to locate the entries), a length value, a base value, and a modify value in the future file (Address Register ARX (x: 0-3), see Fig. 44).

As to claims 16 and 23, Murakami et al.'667 also discloses: said two or more stages include a decode stage ((2) Decode stage

see Fig. 28), an address calculation stage (Address Update stage, see Fig. 28), an execution stage ((4) Execution stage, see Fig. 28), and a write back stage ((5) Write/Accumulation stage, see Fig. 28).

As to claims 17 and 24, Murakami et al.'667 also discloses: the future file (Address Register ARX (x: 0-3), see Fig. 44) is located in the decode stage ((2) Decode stage see Fig. 28) and the data address generator (Adder 534 and 537, see Fig. 44) is located in the address calculation stage (Address Update stage, see Fig. 28).

As to claims 21 and 28, Murakami et al.'667 also discloses: the processor (the Murakami et al.'667's CPU, inherently existing) comprising a digital signal processor (see Fig. 24, and Col. 27, lines 14-15).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

> such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 4, 10, 11, 18, 19, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al.'667 in view of Roth et al. (PUB. No. US 2002/0078326 A1), hereafter referred to as Roth et al.'326.

Murakami et al.'667 discloses the claimed invention except for: storing a committed data address value in an architectural file (in claims 3, 10, 18, and 25); cancelling an instruction in the pipeline; and restoring the future file to a valid state by writing the committed data address value in the architectural file to the future file (in claims 4 and 11); a restore bus connected between the architectural file and the future file; and a control unit operative to write the committed data address values from the architectural file to the future file via the restore bus in response to the pipeline being cancelled (in claims 19 and 26).

Roth et al.'326 discloses: as to claims 3, 10, 18, and 25, storing a committed data address value in an architectural file (32A-C, see Fig. 2 and left Col. at page 2, lines 5-10).

Roth et al.'326 also discloses: as to claims 4, and 11, cancelling an instruction in the pipeline (when the speculation

is not correct and need to be adjusted, see also left Col. at page 5, lines 5-7); and restoring the future file (34A, and 34B, see Fig. 2) to a valid state by writing the committed data address value in the architectural file (32A-C, see Fig. 2 and left Col. at page 2, lines 5-10) to the future file (34A, and 34B, see Fig. 2).

Roth et al.'326 also discloses: as to claims 19 and 26, a restore bus (inherently existing in the Roth et al.'s system) connected between the architectural file (32A-C, see Fig. 2 and left Col. at page 2, lines 5-10) and the future file (34A, and 34B, see Fig. 2); and a control unit (inherently existing in the CPU of the Roth et al.'s system for controlling the data movement) operative to write the committed data address values from the architectural file to the future file via the restore bus in response to the pipeline being cancelled (when the speculation is not correct and need to be adjusted, see also left Col. at page 3, lines 5-7).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Murakami et al.'667's machine to comprise: storing a committed data address value in an architectural file; cancelling an instruction in the pipeline; restoring the future file to a valid state by writing the committed data address value in the architectural file to

the future; and a restore bus connected between the architectural file and the future file; and a control unit operative to write the committed data address values from the architectural file to the future file via the restore bus in response to the pipeline being cancelled, as taught by Roth et al.'326, in order to save the data address values during the speculative process in the events such as exceptions or interrupts therefore to facilitate handling the exceptions and interrupts in the speculative execution and to increase the Murakami et al.'667's processor performance.

Response to Arguments

7. Applicant's arguments mailed 6/12/04 have been considered but are moot in view of the new ground(s) of rejection. As set forth in the art rejections, Murakami et al.'667 and Roth et al.'326 teach the claimed invention.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is

reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the

status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

10. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into

the Group at fax number: 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
September 6, 2004